schematically and which are substituted in Fig. 4 for the illustrated enhancement mode transistors. The transistors and their gate elements are now identified.

The specification page 4, line 21 has been amended by inserting an equal sign (=).

Accordingly, it is believed that the Examiner's objections to the drawings and the specification have been addressed.

Claims 1-17 have been rejected under 35 U.S.C. §103(a) as being unpatentable over applicants' admitted prior art (Figs. 1-4) taken with Brahmbhatt 4,442,481. The Examiner alleges that Brahmbhatt teaches native MOSFETs are recognized as equivalent to enhancement mode MOSFETs but have a very low threshold voltage that does not require additional doping; therefore, unwanted manufacturing variations are reduced. The Examiner concludes that the use of native transistors in the transconductance cell of Fig. 4 would be a mere substitution of art recognized equivalent MOSFETs.

This rejection is respectfully traversed. The invention is directed very specifically to a transconductance cell for use in a system on a chip to reduce adverse effects of bulk semiconductor voltages on transconductance. As noted in the background in the invention on page 2, line 15 et. seq., a problem with the use of the known transconductance cell as shown in Fig. 4 lies in adverse effects of source-bulk voltage (VSB) on MOS transistors used in the transconductance cell. Variations in VSB due to bulk (chip) stray voltages can adversely affect transconductance. Further, control voltage in a gyrator can have a limited dynamic range when using conventional enhancement mode MOS transistors.

The problem is addressed through use of native transistors in the transconductance cell in place of the conventional enhancement MOS transistors, which leads to a lower variation of GM due to source to bulk voltage variations. Heretofore, this problem with the use of known transconductance cells employing conventional enhancement MOS transistors has been endured without any proposed solution. The

present invention offers this solution and provides for an improved transconductance cell for use in a system on chip to reduce adverse effects of the bulk semiconductor voltages.

Applicant does not claim to have invented the native transistor, which it is admittedly well known as evidenced by the cited Brahmbhatt patent. However, Brahmbhatt is concerned with a low power decoder circuit, and Brahmbhatt suggests the substitution of native transistors for conventional transistors since the native transistors do not require channel doping and thus eliminates a process step. Note column 9, lines 10-19 where Brahmbhatt describes that no additional doping is necessary to create the channel region, i.e. the native semiconductor material is used. This differs from the standard enhancement and depletion mode FETs discussed previously in that they do require doping to alter the conductivity of the channel region. According to Brahmbhatt, the advantage of using the native device rather than a depletion mode transistor lies in the fact that variations in the manufacturing process will sometimes cause a depletion mode transistor to have a deeper channel than desired.

Accordingly, it is seen that Brahmbhatt is using native transistors solely for process considerations. Brahmbhatt is not concerned with variations in source-bulk voltage due to bulk stray voltages which adversely affect transconductance. This is a problem particular to use of a transconductance cell in a telecommunications receiver system on a chip to reduce adverse effects of bulk semiconductor voltages.

This is not shown or suggested by Brahmbhatt who is concerned with a low power decoder circuit and manufacturing processes.

Accordingly, it is respectfully submitted that claims 1-17 as amended are patentable over the admitted prior art taken with Brahmbhatt.

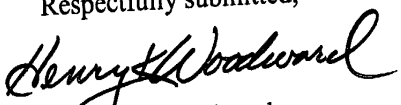
The art cited but not applied by the Examiner has been reviewed and is not made relevant to the invention as defined by claims 1-17 as amended, drawn to a transconductance cell for use in a telecommunications receiver system on a chip.

Since the objections to the drawings and the specification have been addressed, and since claims 1-17 as amended are patentable under 35 U.S.C. §103(a)

over the admitted prior art taken with Brahmbhatt, all as above as set forth, it is requested that claims 1-17 as amended be allowed and the case advanced to issue.

Should the Examiner have any questions concerning the present amendments, a telephone call to the undersigned attorney is requested.

Respectfully submitted,



Henry K. Woodward
Reg. No. 22,672

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: (415) 576-0300
HKW:ejt
PA 3254631 v1

## VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Rewrite the paragraph on page 2, lines 4-8.

--Filter elements in the system require inductive elements such as shown in Fig. 3A. Since inductors are difficult to realize in integrated circuits and systems, a functional equivalent inductive element, or gyrator, has been devised. As shown in Fig. 3B, the gyrator comprises variable transconductance elements, GM, serially connected with a shunt **[compacitance]** capacitance, C.--

Rewrite the paragraph on page 2, lines 15-19.

--A problem with the use of the known transconductance cell lies in adverse effects of source-bulk voltage (VSB) on MOS transistors used in the transconductance cell. Variations in VSB due to bulk (chip) stray voltages can adversely affect transconductance. Further, control voltage in a gyrator can have a limited dynamic range when using conventional enhancement MOS transistors.--

Rewrite the paragraph on page 2, lines 26-29.

--A feature of the invention is the use of native transistors in the transconductance cell. The native MOS transistor has a lower threshold voltage Vt than the conventional enhancement MOS transistor, which leads to lower variation of GM due to source to bulk voltage variations.--

Page 3, after line 19, insert the following new paragraph:

--Fig. 9 is a schematic of native transistors as used in a transconductance cell in accordance with the invention.--

Rewrite the paragraph at page 3, line 29 through page 4, line 5:

-- Fig. 6 is a schematic of Vco 42 implemented as a second order harmonic oscillator including cross coupled transconductance cells 52, 54, and capacitors 53, 55 and a non-linear resistor 56. As noted above, the control voltage generated by ring oscillator of Fig. 5 is used to control the transconductance, GM, stages within the filter and hence the cutoff frequency of filters 24, 25. Each transconductance cell or GM stage can be identical schematically to the transconductance cell shown in Fig. 4 including transistors 3 and 4 having gates 5 and 6, respectively, within circle 60. The circled transistor devices shown at 60 in Fig. 4 function as load resistors for current sources 62, 64 which are serially connected with current sources 63, 65 to provide two outputs Out P and Out N of the transconductance device. Block 66 is a voltage common mode feedback for the current sources, the details of which are known and not described further herein.--

Page 4, line 20-24, rewrite **Equation 2** as follows:

$$--Vt=Vt0+\gamma((\sqrt{2}|\varphi F|+VSB)- +(\sqrt{2}|\varphi F|)) \qquad \textbf{Equation 2}$$

Where $Vt0=Vt(VSB=0)$,

$\gamma$ Is the bulk threshold parameter ($\sqrt{}$volts)

$\varphi F$ is the strong inversion surface potential (volts)

VSB is the source to Bulk Voltage.--

Rewrite the paragraph at page 4, line 30 through page 5, line 12:

--As noted from Equation 1, the threshold voltage, $V_t$, of the MOS transistors affects the transconductance. In accordance with the invention the use of a low to zero threshold voltage transistor, a "native" device, improves the filter performance in the presence of substrate noise. The native transistors 3',4' shown schematically in Fig. 9 are used in the transconductance cell of Fig. 4 in place of

conventional enhancement mode transistors 3,4. As is well known in the semiconductor art, a "native" transistor does not have threshold adjusting dopants in the channel region as in conventional MOS transistors. The $V_t$ of a native device used with the transconductance cell of Fig. 4 is a 0.041 volt has a saturation current, $I_{sat}$ of 5.83 mA. Although the $V_t$ of the native device has a similar dependence on VSB as does the conventional MOS transistor, its low absolute value with respect to a Vgs of approximately 500 mV, means that the overall transconductance does not vary much with VSB. Figs. 7A, 7B illustrate transconductance variance with varying VSB with a native transistor load and with a standard MOS transistor load, respectively. Fig. 7B is the small signal transconductance variance due to ± 100 mV VSB using a standard MOS arrangement, whereas Fig. 7A is GM variance using the native MOS transistor. It is noted that the native MOS transistor provides a variance of ± 0.3% up to 1 MHz, whereas the standard MOS transistor has a variance of ± 9.7% over the same frequency range.--

IN THE CLAIMS:

Rewrite claims 1 and 7 as follows:

1. (Amended) A transconductance cell for use in a telecommunications receiver system on chip to reduce adverse effects of bulk semiconductor voltages on transconductance comprising a plurality of current sources interconnected to provide an output transconductance control voltage, and a variable load for the current sources including first and second load resistors each serially connected with one of the plurality of current sources, and a variable resistance interconnecting nodes of the load resistors, the variable resistance comprising a pair of native MOS transistors having low threshold voltages.

7. (Amended) The transconductance cell as defined by claim 4 wherein the system on a chip comprises a radio receiver, and the transconductance cell is used in a voltage controlled oscillator.